Martin C. Alcock, M. Sc. (Dist),
Technology Professional

An experienced technology professional with skills in a several application areas including, embedded systems and FPGA design, Digital Signal Processing and client/server. Experienced in high speed computing, and domain knowledge in the telecommunications, RF and digital cable spaces. Self-motivated entrepreneur and manager with a history of several completed contracts and projects, and has built a successful consulting practice over the last 10 years.

Technical abilities: Embedded Systems and FPGA

Real time system design ● Xilinx Vivado ● Altera Quartus II/Open CL
VHDL ● Verilog/System Verilog ● Schematics/Layout ● Board turn/up
ARM Cortex embedded processors ● Altera NIOS II ● Xilinx Microblaze
Ethernet on Silicon ● OpenCL in C ● Java based FPGA design

Technical abilities: Digital Signal Processing

Cellular telephony ● Modulation and Demodulation ● Filtering ● Integration
Sonar processing ● FFT ● QAM/QPSK ● OFDM ● GPS/DGPS
Sub-sampling ● Interpolation and Decimation ● Encryption/Decryption
MPEG Compression ● MPEG Stream splicing

Technical abilities: Client/Server Applications

Software Engineering ● OO Design ● UML ● Software Quality Assurance
Programming in C/C# /C++/Java ● ASP.NET ● Agile Development ● MySQL
Network programming ● TCP/IP ● Stack design ● Performance tuning
Windows Applications ● Unix/Linux Applications ● Web based Applications
CVS/SVN Revision Control ● Code reviews

Management Skills

Team Building ● Motivation ● Problem solving
Project Planning ● Management Reporting ● CXO Level Presentations
Startup Companies ● Entrepreneurship ● Mentoring ● Business Planning

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Testimonials and endorsements:
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Projects and work history

March 2011 to Present, Consulting Practice
dba Praebius Communications Inc (Founder and Principal)

Mobile Digital Video Monitoring Application (December '16 to present)

- Participated in an FGPA based mobile video project for a military vehicle
- Implemented analog to digital input modules for a variety of formats in Verilog on Arria 10 FPGA
- Created custom peripherals based on AXI Lite bus in Verilog
- Participated in design of text overlay system

DSP based OFDMA Receiver (September '16 to December '16)

- Modelled a DOCSIS 3.1 Fine ranging receiver using the C language
- Built an OFDMA equalizer and demodulator using Xilinx Microblaze embedded processor
- Added logic in VHDL to manage buffering, and post-demodulation processing

UDP Offoading Engines in FPGA (May '16 to September '16)

- Contributed to a team development effort for a bespoke UDP offloading and multiplexing engine in Verilog
- Created front end parsing and rules based routing logic

Heterogeneous Development Environment project (September '15 to May '16)

- Designed and implemented a system for designing heterogeneous computing systems using an unified source in the Java language (Java CL)
- Implemented a Java bytecode to C language translator to target FPGA compilers
- Generated a plug-in for the popular Eclipse development environment to enable compiling for an FPGA in a unified environment
- Built support packages for system on chip FPGAs using embedded Linux (Yocto) on ARM Cortex (Altera Cyclone/Xilinx Zync) and specialized device drivers
- Packaged product and rolled out a web site for participants (www.javacl.org)
- Demonstrated several applications on an SOC prototyping board

Other short term contract work (2011-2017)

- Launched a product for a security application based on Android, ASP.NET and MySQL technologies
- Designed and implemented a mobile application on Android platform in Java
- Developed numerous websites using ASP.NET and C# and MySQL databases
- Designed coverage estimates for small buildings and Installed 802.11 wireless networks using commercial access points
- Installed PBX system in a small office and several Cat5 wired Ethernet systems

Derivative Work from Master of Science thesis

- Heterogeneous computing in Java with JOP and logic
- Created an FPGA based MPEG transport stream splicing technology
- Built FPGA based MPEG splicing engine in Verilog
- Implemented embedded Java engine (JOP) and ported C++ to Java
- Implemented minimal TCP/IP stack on target processor in Java

Independent Research and development projects (ongoing)

- Invented a novel power-saving FFT implementation using negabinary complex arithmetic, prototyped on an FPGA using VHDL
- Published paper on FFT work, also patent pending
- Amateur Radio repeater controller on a MAX 10 FPGA
- YAFOE – Yet another FPGA Offload Engine: an FPGA implementation of a YACC parser for protocol parsers defined in BNF grammar.
- DSPGEN – a tool for generating DSP structures on an FPGA in Verilog using the Lossless Discrete Integrator (LDI).

March 2013 to September 2015, Senior Consulting FPGA Engineer
SRC Computers, LLC, Colorado Springs, Colorado
Consultant with Oxford Global Resources

High speed Ethernet system (March '13 to September '15)

- Designed and implemented several high speed Ethernet front ends for a supercomputer using several NIOS embedded processors on an Altera Stratix IV FPGA
- Coded low-level drivers for hardware components on a NIOS processor and wrote system diagnostics in C++
- Implemented hardware assisted UDP offloading logic to enable high speed traffic in a NIOS environment by intercepting MAC traffic
- Designed and implemented a Content addressable memory (CAM) and implemented a hardware assisted buffering scheme

March 2012 to March 2013, Contract FPGA Engineer
Vecima Networks Inc, Saskatoon, SK
dba Praebius Communications Inc

Cable Head End contract work (March '12 to March '13)

- Implemented new features for MPEG transport packet processing on an existing Xilinx Virtex 5 design in Verilog
- Designed and implemented Ethernet subsystems for offloading UDP packets on a Linux-based Power PC in an FPGA
- Simulated and verified design of a large cable head end ASIC in Verilog using ModelSim, captured data for further analysis

July 2006 to April 2011, Chief Technology Officer
2008-2011 Ad Systems Communications Inc, Salem Oregon
2006-2008 Ad Systems Inc, Murray Utah
dba Praebius Communications Canada LLC

- Designed digital ad insertion and playback software for small cable head ends using MPEG-2 playback on Windows that ran in real time
- Ported server code to an Ubuntu Linux platform
- Designed an internet based cue redistribution system using TCP/IP and UDP
- Implemented head end for insertion system on Windows Server platform in C/C++
- Created a traffic and billing system using a novel cloud computing model using ASP.NET, C# and MySQL on Windows Server
- Managed the deployment and turn up of 100+ field inserters
- Built a custom MPEG 2 playback system on an FPGA
- Filed US patent application 12,287,793 as co-inventor

Sept 2001 to March 2006, Founder, Director and CEO
Integen Technologies Inc

- Created a custom cable-based 802.3 delivery technology for small hotels based using a microcontroller and home grown cable modem
- Implemented microcontroller code in real time using embedded C
- Implemented modulation/demodulation code on Xilinx Virtex FPGA using VHDL
- Developed Ethernet-to-cable algorithms for head end modem, including congestion and windowing algorithms
- Built a custom video on demand system as an overlay to 802.3 system
- Led a multi-disciplinary team in hardware, software and industrial design

November 1997 to August 2001, ***Senior Manager***
WiLAN Inc

- Conceived the architecture for an FPGA-based 802.16 (WiMAX) wireless transceiver
- Participated in working group for the WiMAX and G4 (LTE) cellular standards
- Led a multi-disciplinary development team to deliver this and other products in the roles of line and project manager, and lead architect.
- Implemented an embedded FFT algorithm on single Xilinx 4000 series FPGA.
- Absorbed other engineering groups, which included similar products on DSP based platforms.
- Promoted to a senior engineering management role and my successor continued my work to roll out an ASIC based version as well.
- Wrote applications for SR&ED credits, as well as ITC and IRAP funding

Further experience for the years 1975 to 1997 are available on request.

Accomplishments

- **Implemented** an LR parser on an FPGA for protocol parsers, including a Verilog based parsing algorithm. Novel use of an existing compiler technology.
- **Created an abstraction** of Open CL in the Java language to simplify rollout of SOC based systems, prototyped applications and rolled out a website for participants (www.javacl.org)
- **Published a minimal logic FFT algorithm** based on negabinary complex numbers, a numbering system based on the square root of -2.
- **Designed a MPEG splicing technology** based on an embedded native Java processor in an FPGA. Demonstrated real time performance.
- **Created a networked Ad insertion system** for cable television, in both analog and digital domains. Patent pending.
- **Invented and developed a system for tracking bus passengers** by combining wireless and RFID technologies together, patent pending.
- **Created a video on demand system** and rolled out a pilot program. Patent granted for a unique approach to delivering media to rooms which was based on a home grown delivery technology implemented in a processor and FPGA.
- **Led the development of an FPGA/ASIC based OFDM transceiver** delivered the first market-ready consumer product and platform for future products. Led the development as architect, line and project manager of a large engineering group.
- **Launched a program for a credit card size DGPS receiver** shrinking an existing product by a factor of 5 and cost by a factor of 10 by re-implementing a design in single DSP processor using zero IF demodulation.
- **Created a rapid prototyping tool** for DSP system designs called ‘EZDSP’, including a language compiler, coefficient generator and software oscilloscope.
- **Invented** a novel scheme for communicating with through a pipe wall by modulating a magnet with coherent FSK. Invention included a novel and proprietary FM demodulator using PSK.
- **Designed** a state machine processing engine to control a radio repeater, including timeout and DTMF control. Built a discrete component, CPLD and fully integrated FPGA version. Featured publication in an Amateur Radio magazine.
- **Discovered a novel method for pipe wall profiling** by using a DFT algorithm as a demodulator, implemented on a DSP and FPGA. Deployed to profile riser pipes in the North Sea.
- **Implemented a π/4 QPSK modem for digital cellular** on a single Xilinx FPGA without multipliers.
- **Patented** a scheme for timing adjustment in raised cosine FIR filters by interpolating the filter coefficients in conjunction with two colleagues.
- **Directed an ASIC program for a cellular phone and** delivered both the ASIC and the phone to market as technical project leader, and architect.
- **Earned an M. Sc. Degree** in Software Engineering with Distinction, thesis work received dissertation of the year award.

Patents

Receiver having an adjustable matched filter

United States Patent 5,309,482

Inventors: Martin Alcock, Theo Smit, Andrew Wright

A method of achieving timing adjustment in a digital receiver by interpolating matched filter coefficients, thus eliminating the need for external hardware.

Networked Ad Insertion System

United States Patent Application 12,287,793

Inventors: Martin Alcock, Bob Hall

A system that distributes insertion cues over the internet, enabling lower cost head ends that do not receive cues to participate in ad insertion.

Publications

"IDE for Analog Devices EZ-Kit LIte" Analog devices DSPatch number 34, Fall 1995. Overview of EZDSP project.

"An object oriented methodology for the analysis and design of real-time mixed mode systems" M. Sc. Thesis, University of Liverpool, UK.

"Design of a power-reduced FFT for OFDM transceivers using negabinary arithmetic" In progress as an IEEE publication.

"FPGA based repeater controller" A controller for an amateur radio repeater using a state machine engine and Goertzel algorithm for DTMF tone detection. CQ Ham Radio magazine, December, 2016.

Education and Citizenship

Master of Science in Software Engineering, University of Liverpool, United Kingdom, and Degree was awarded with distinction. Dissertation topic was an object oriented methodology to implement real time systems on an FPGA using a combination of embedded controllers and logic, which achieved the Dissertation of the year award.

Dual citizen of both Canada and United Kingdom, and holder of valid passports for both countries and entitled to work in Canada, the European Union and the United States (under a TN Visa). Also screened by US and Canadian customs as a member of the NEXUS trusted traveler program.

References

Available on request.

Hobbies and other interests

Licensed Amateur radio operator, private pilot for small single and dual engine aircraft under 12,500 lbs, certified Scuba instructor and member of PADI. Also an Amateur Symphonic Conductor, interested in classical and baroque music.